TITLE OF THE INVENTION

VIDEO FIELD RATE PERSISTENCE

BACKGROUND OF THE INVENTION

The present invention relates to the display of video waveform data, and more particularly to a video field rate persistence for the video waveform data to eliminate flickering.

In certain field rate video displays on a video waveform monitor, such as a component video parade display, it is not cost effective to update each parade element (video component) on every field output to the video waveform monitor. Therefore the displayed field rate waveform parade appears to flicker due to each parade element being alternately and separately displayed once during each consecutive field. For instance in a field rate RGB display the R parade element is displayed in the first third of the display during fields N, N+3, N+6, etc., the G parade element is displayed in the second third of the display during fields N+1, N+4, N+7, etc., and the B parade element is displayed in the last third of the display during fields N+2, N+5, N+8, etc.

Besides causing display flicker, the temporal separation between the various parade elements and overlay elements in field rate displays makes it difficult to perform a coherent "screen capture" for use in hardcopy or web interface applications since only one of the elements is displayed per field interval or display cycle.

What is desired is a means for alleviating the display flickering and temporal separation of multiple elements in a video waveform monitor display which updates at a field rate.

BRIEF SUMMARY OF THE INVENTION

Accordingly the present invention provides a video field rate persistence for alleviating display flickering and temporal separation of multiple components on a video waveform monitor by providing a per pixel persistence lasting for X fields, where X is usually set to the number of the multiple components. A persistence count is assigned to each pixel which indicates the number of fields since the pixel was updated. When a new pixel value for one of the elements is input or the persistence count is maximum, the persistence count is reset to zero and the new pixel value replaces the previous pixel value for that component. The other components have their persistence count incremented and the previous pixel value is rewritten as the current pixel value for those components. In this way for each field when the display is updated, all of the components are displayed rather than just the one for which new pixel values are received.

The objects, advantages and other novel features of the present invention are apparent from the following detailed description when read in conjunction with the appended claims and attached drawing.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

Fig. 1 is a block diagram view of a waveform monitor having video field persistence according to the present invention.

Fig. 2 is a block diagram view of a circular field buffer with video field persistence according to the present invention.

Fig. 3 is a plan view of a video waveform monitor screen illustrating the effect of the video field persistence according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring now to Fig. 1 a waveform monitor **10** receives a serial digital video signal at an input of an input processor **11**. The input processor **11** provides for cable equalization, reclocking and serial-to-parallel conversion so that the output from the input processor is in the form of parallel video components **Y, Pb, Pr**. The parallel video components are input to a rasterizer **13** that rasterizes one complete field of each video component into a separate bit map, sequentially one incoming field at a time. The resulting bit maps are sent to a circular field buffer **16** with a persistence algorithm **12** as described below. For example for sequential bit maps, bit map 1 has the **Y** component of incoming field 1, bit map 2 has the **Pb** component of incoming field 2, bit map 3 has the **Pr** component of incoming field 3, bit map 4 has the **Y** component of incoming field 4, . . . bit map N has the **Pr** component of incoming field N. In the bit map the Y-axis represents the selected component value, the X-axis represents time (corresponding to one video line) and the Z-axis represents intensity (the sum of overlayed pixels for all of the video lines of a particular field). The output from the circular field buffer **16** is a display raster for a**18** display, the display raster being divided into sub-buffers, one for each separate video component.

As shown in Fig. 2 new pixel data for display from the latest bit map output by the rasterizer **13** is input to the persistence algorithm **12** within a digital signal processor (DSP) **14**. A previous pixel from the circular field buffer **16** also is input to the persistence algorithm **12**. Output from the persistence algorithm **12** is a resulting pixel that is input to the circular field buffer **16**. Each field the circular field buffer **16** provides the display raster to

the video waveform monitor display **18**, which is the combination of the sub-buffers. The display raster represents the current bit map input to the circular field buffer **16** as well as the previous two bit maps which are stored in the respective sub-buffers of the circular field buffer according to the persistence algorithm **12**, as explained in detail below.

The persistence algorithm **12** is described by the following description:

if (Pixel_Persistence_Count(Previous_Pixel) = Maximum_Persistence(X)

or

New_Pixel ≠ 0

or

Previous_Pixel = 0)

then

Pixel_Persistence_Count(Resulting_Pixel) = 0

and

Resulting_Pixel = New_Pixel

else

Pixel_Persistence_Count(Resulting_Pixel) = Pixel_Persistence_Count(Previous_Pixel) + 1

and

Resulting_Pixel = Previous_Pixel

In other words for a video component parade display if the current field or bit map N input to the circular field buffer **16** has **Y** component parade element data, then X=2 ($0 \leq X \leq 2$) and the new pixels are provided for the first one-third of the display raster and are zero for the other two-thirds of the display raster. The persistence count for the **Pb** component parade element pixels is one (corresponding to bit map N-1), for the **Pr** component parade element pixels is zero (corresponding to bit map N-2), and for the **Y** component parade element pixels is two. Since the previous pixels from the **Y**

component parade element have a persistence count of two, i.e., maximum, the persistence count is set to zero for the resulting pixel and the resulting pixel value is set to the new pixel value for the **Y** component parade element pixel in the first third of the display raster. For the **Pb** and **Pr** component parade element pixels in the second third and last third of the display raster the persistence count is not maximum and the new pixel values are zero, so the persistence count is incremented and the resulting pixel is set to the previous pixel value, i.e., there is no change in the **Pb** and **Pr** component parade element pixel values in the last two-thirds of the display raster. Thus the display **18**, as shown in the Fig. 3 screen shot, shows the new **Y** component parade element pixels in the first third of the display raster and the previous **Pb** and **Pr** component parade element pixels in the last two thirds of the display raster.

Although the above is described in terms of **Y**, **Pb** and **Pr** video components, it is applicable to any other multiple video component display, such as **RGB**, with the maximum persistence count being equal to the number of components being displayed. Also the persistence count may be decremented rather than incremented, starting from the maximum persistence count and updating at a zero persistence count.

Thus the present invention provides a video field rate persistence by repeating pixel values in a display raster for video components that are not being updated during a particular field interval being displayed.